

Analysis of a Soliton-Based Logic Module for a Ring Network

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Abstract— We analyze and numerically study the code-matching logic module that is the central element in a proposed soliton-based ring network system running at peak rates of 100 Gb/s. The proposed network is packet-switched, and fast logic is required to route each packet. That is the function of the code-matching logic module, and four soliton logic gates that can perform fast logic are the key devices in its design. The behavior of the code-matching logic module is governed by a large set of parameters, and we simulate it by varying many of these parameters. The physical effects that occur in these devices and their significance are analyzed. The results indicate that the logic module will work but within a restricted parameter range.

I. INTRODUCTION

INTERACTIONS between soliton pulses traveling along the two polarization eigenaxes in a birefringent fiber results in frequency and time shifts of the two pulses due to cross-phase modulation and can even lead to mutual self-trapping [1]. This physical effect can be used to carry out all-optical switching and is the basis for the soliton dragging and trapping gates that were invented by Islam *et al.* [2]. Sauer *et al.* [3] have proposed a soliton ring network based on soliton logic gates with a 40 Gb/s payload data rate, 1.25 GHz packet rate, 100 Gb/s peak bit rate, and 254 users. The network may span several tens or hundreds of kilometers. To operate at such high bit rates, solitons must be used to avoid the harmful effects of group-velocity dispersion and self-phase-modulation. The soliton ring network uses digitally encoded, self-routed packet switching. Soliton dragging and soliton trapping gates are used to decode the header accompanying each data packet at the network access nodes. Using all-optical gates increases the switch bandwidth which in turn increases the average bit rate available to each user. The design is a feed-forward

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architecture that exploits bandwidth while downplaying the latency of the ultrafast logic gates.

The self-routing packet has 42 b with 32 b for data and 10 b for the header. In the header, 8 b indicate to the address, one bit is used for synchronization, and the remaining bit is used for packet cleanup. An empty packet has all its eight address bits set to 1 to simplify empty-packet detection and to maintain synchronization.

A complete simulation of the full 256-node network is impractical at present. Although it may be possible in the long term to address this issue through the use of reduced models [4], [5], we focus here on complete simulations of the code-matching logic module that is at the heart of each node.

The code-matching logic module is used to decode the eight bit address—both to determine if the packet address matches the node address, in which case the packet should be removed from the ring, or if the packet is empty, in which case the node can insert a new packet. This code-matching logic module must operate at the bit rate, in contrast to the other processing elements in the node that can operate at the much slower packet rate. It consists of four all-optical soliton logic gates, while the rest of the network only contains electronic gates.

In this paper, we carry out complete simulations of the code-matching logic module, in which we solve the full set of partial differential equations that describe light propagation in the gates. The purpose is to determine optimal parameters for the module's operation and the sensitivity of its operation to parameter variations. As will become apparent, there is a large parameter space to explore, and we must make reasonable choices in exploring this space. With this caveat, our results indicate that it is possible to find a parameter regime within which this device can operate successfully, but this parameter regime is quite narrow.

The remainder of this paper is organized as follows. In Sections II and III, we review the operation of the soliton logic gate and the code-matching logic module. In Section IV, we discuss the key design issues. In Section V, we present our simulations. Section VI contains the conclusions.

II. OPERATION OF SOLITON LOGIC GATES

The basic operation of a soliton logic gate is shown schematically in Fig. 1. The arrows on the signal and control pulses indicate motion relative to the central group velocity frame. When two orthogonally polarized pulses undergo a partial collision in a birefringent fiber, the two pulses interact nonlinearly through cross-phase-modulation which leads to a shift

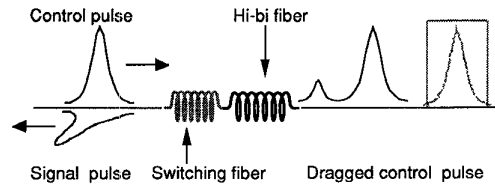


Fig. 1. Schematic illustration of a soliton logic gate.

in frequency of both pulses that tends to reduce their velocity difference. In particular, when the signal pulse shown in Fig. 1 is present, then the velocity of the control pulse changes, while in the absence of the signal pulse the velocity of the control pulse does not change. In the second length of highly birefringent fiber, the velocity shift translates into a time shift, allowing one to switch the control pulse out of its timing window. It is desirable to use two different fibers because the birefringence must be low enough in the first fiber so that pulses have a significant nonlinear interaction. As a consequence of the low birefringence, it is difficult to maintain polarization. Maintaining polarization is crucial for the gate to operate properly and is, in fact, a key experimental difficulty. When the pulses are no longer interacting, and low birefringence is no longer necessary, it is therefore desirable to use high birefringence fiber to minimize polarization-mixing. These switches are cascadable because the control pulse becomes the signal pulse for the next stage, while the former signal pulse is discarded, and fan-out is achieved because the signal pulse can have far less energy than the control pulse. We note, however, that the design of the code-matching logic module [6] requires an XOR gate in which the signal pulse is combined with the control pulse rather than being discarded, thus limiting the cascability of the device.

Islam *et al.* [2], [7], [8], who invented the soliton logic gates, have shown in a series of experiments that they can operate at a switching energy as low as 1 pJ and can operate with pulse durations of 500 fs [9], corresponding to a theoretical operating bit rate of 0.2 THz, assuming an inter-pulse spacing of 10 times the pulse duration. We note, however, that these low energies and short pulse durations have not been achieved simultaneously. These gates are logically complete. They do, however, have very long latency, typically microseconds, due to the long length of the second fiber that is required to translate the frequency shifts into time shifts.

There are two different kinds of soliton logic gates. In the first kind, referred to as dragging gates, the velocity of the control pulse changes when interacting with the signal pulse, but ultimately the two pulses separate. In the second kind, referred to as trapping gates, the velocity shift is sufficient to lock the signal pulse and the control pulse together. Both are used in the code-matching logic module. Trapping gates are used at the end of the module since the frequency shift is particularly large in these gates, and use of a frequency discriminator allows one to convert a time-shift-keyed signal into an amplitude-shift-keyed signal which can then be converted into an electronic signal.

Our entire discussion up to this point has been premised on the assumption that the signal and control pulses can be

treated as single, uniform lumps—essentially solitons. In fact, these gates operate in a regime in which these pulses are far from ideal solitons and undergo a complex evolution in which their shapes can change, in which they can radiate, and other difficult-to-characterize behavior can occur. The central purpose of this work is to track this complex evolution as the pulses propagate sequentially through the gates that form the code-matching logic module. We can then determine how the real-world evolution degrades the expected performance of the device, and we can optimize the performance within the parameter space that we examine.

The full evolution of the pulses in these gates is governed by the coupled nonlinear Schrödinger equation [1], [6] that may be written in normalized form as

$$\begin{aligned} -\left(i\frac{\partial u}{\partial \xi} + i\delta\frac{\partial u}{\partial s}\right) &= \frac{1}{2}\frac{\partial^2 u}{\partial s^2} + \left(|u|^2 + \frac{2}{3}|v|^2\right)u, \\ -\left(i\frac{\partial v}{\partial \xi} - i\delta\frac{\partial v}{\partial s}\right) &= \frac{1}{2}\frac{\partial^2 v}{\partial s^2} + \left(\frac{2}{3}|u|^2 + |v|^2\right)v \end{aligned} \quad (1)$$

where u and v are the pulse envelopes along the two polarization eigenaxes, s is normalized time, ξ is normalized distance, and δ is normalized birefringence. The magnitude of the cross-phase modulation is 2/3 that of self-phase modulation because the fiber is assumed to be linearly birefringent. The terms on the right-hand side include the effects of group-velocity dispersion, self-phase modulation, and cross-phase modulation. Pulses in orthogonal polarizations create a mutually attractive potential well through cross-phase modulation, and this coupling mechanism is independent of the phase between the two pulses. Linear birefringence is included through the terms with the coefficient $\delta = \pi\Delta n(\tau/1.76)/\lambda^2|D|$, where D is the dispersion in ps/(nm-km) and Δn is the index difference between the two principal axes. A characteristic length for propagation in the fiber is the soliton period $Z_0 = 0.322\pi^2 c\tau^2/\lambda^2|D|$.

We solved these equations using the standard split-step Fourier transform method [1].

III. CODE-MATCHING LOGIC MODULE

We show a schematic illustration of the code-matching logic module (CMLM) in Fig. 2. The CMLM contains four soliton logic gates referred to as G_1 , G_2 , G_3 , and G_4 , and the physical type of each gate is marked in Fig. 2 under the gate. The CMLM operates on each packet header that passes through the node in order to carry out two logically separate functions. The first is to determine if the packet header matches the local address or code. If so, then the packet should be retrieved from the ring. The second is to determine if the header consists of all logical 1's in which case the packet is empty. If so, the node can put a packet onto the ring. The header bits are designated by the symbol H in Fig. 2, and the code bits are designated by the symbol D . The clock inputs, which are required to both select the header bits from the other packet bits and to act as the control pulse in gates G_1 , G_3 , and G_4 , are designated C_1 , C_3 , and C_4 . They are logically identical but are physically distinct and are therefore labeled separately. One important physical difference is that

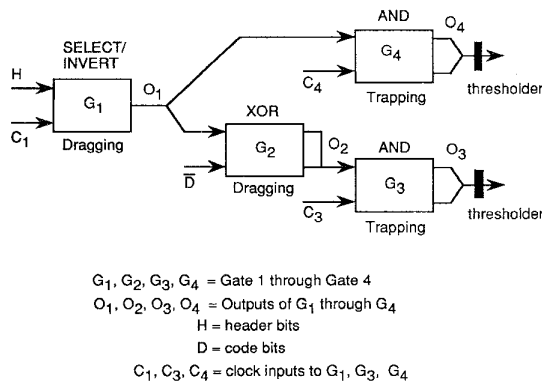


Fig. 2. Schematic illustration of the code-matching logic module that is used at every node to decode the header. The logic operation that each gate carries out is marked above the gate, and the physical gate type is marked below. The clock inputs C_1, C_3 , and C_4 are all logically identical but can be physically different and are separately identified. The purpose of each gate is summarized in Table I.

they must be timed separately because of the large gate-to-gate propagation delays. The output of the gates are labeled O_1, O_2, O_3 , and O_4 .

We will use the symbols $C_1, C_3, C_4, O_1, O_2, O_3, O_4, H$, and D to indicate both the physical pulses and their logical values, so that when we write $H = 1$, we mean that a particular header bit has a logical value of 1, but when we write that H is a single pulse in the timing window, we mean that a particular header bit consists physically of a single pulse in the timing window. The relationship between the logical values of the variables and their physical representations is not unique. A logical 1 corresponds to one or more physical pulses of which at least one is in the timing window, while a logical 0 corresponds to either the absence of a pulse or one or more pulses outside the timing window. This point bears emphasis because a logical 0 is often created by shifting an entire pulse outside the timing window, and the failure of one of the pulses to shift entirely outside the timing window is one of the principal failure modes of the CMLM.

We show the purpose of each gate and the logical operation that it is expected to carry out in Table I. The purpose of the first gate G_1 , which is a dragging gate is to select the 8 b header, perform timing restoration, and invert the header bits. The clock C_1 is used to select the header bits by setting $C_1 = 1$. The purpose of the second gate G_2 , which is also a dragging gate, is to determine whether each header bit matches the corresponding code bit of the local node's address. Finally, if there is a match, then the trapping gate G_3 transmits no energy to the threshold. If the final output for the 8 sequentially processed header bits is 0 then the packet belongs to the local node. The gate G_4 transmits no energy to its threshold if $H = 1$. Again, if there is no energy transmitted by G_4 for all 8 bits in the header, then the packet is empty and can be replaced. The gates G_3 and G_4 are not logically necessary but serve, together with the thresholds, as optical-to-electronic convertors.

In the original design of the soliton dragging gates, the former signal pulse is discarded after passing through the second length of the fiber by use of a polarizing filter,

TABLE I
THE LOGICAL OPERATION CARRIED OUT BY EACH GATE AND ITS PURPOSE IS SUMMARIZED

Gate	Logical Operation	Purpose
G_1	$C_1 \cdot \bar{H}$	To select the header bits and invert them
G_2	$\bar{O}_1 \oplus \bar{D}$	To determine whether the header and the code (local address) match
G_3	$\bar{O}_2 \cdot C_3$	If the header and the code match, then no energy is transmitted to the threshold
G_4	$\bar{O}_1 \cdot C_4$	If the header contains all 1's (empty packet), then no energy is transmitted to the threshold

while the polarization of the former control pulse is switched, and it becomes the signal pulse in the next stage [2], [6]. This logic achieves cascability by ensuring that no pulse propagates through more than two gates. However, in order to physically implement the XOR logic in gate G_2 , one must combine the signal pulse with the control pulse at the output with an appropriate temporal offset once the control pulse's polarization has been switched. Since the control pulse in G_1 is C_1 , we see that the physical pulse corresponding to C_1 actually propagates through the entire three-gate sequence $G_1 \rightarrow G_2 \rightarrow G_3$. Thus, noise effects can accumulate throughout this entire sequence, and the pulse can also distort significantly due to pulse-to-pulse interactions.

The CMLM consists of two logically independent sequences $G_1 \rightarrow G_2 \rightarrow G_3$ and $G_1 \rightarrow G_4$ which implement respectively the two functions of the CMLM. These two sequences may be studied separately, and in this work we will concentrate on the former sequence. This sequence is more complex, both because it contains three gates, rather than two, and because it contains the XOR gate whose behavior, as previously mentioned, is somewhat more complicated than standard soliton gates. Thus it is more difficult to find a parameter regime in which the three-gate sequence works than to find a parameter regime in which the two-gate sequence works.

We assume that $C_1 = C_3 = C_4 = 1$ so that a header bit is selected. There are four possible logical combinations of the header bit H and the code bit D . In this work, we will simulate these four cases and determine system parameters that optimize the physical contrast ratio between a 1 and a 0. Focusing on a single bit is sufficient for our purposes as the code-matching logic module is designed to process all the packet bits sequentially. An optical amplifier can be added to the output of the module so that the magnitude of the output will be large enough to overcome noise in the following electronics if necessary.

The ideally expected logical behavior is summarized in Table II for each of the four cases, and a schematic illustration

TABLE II
THE EXPECTED OPERATION OF EACH GATE IN ALL OF THE POSSIBLE CASES.
THE INPUT AND OUTPUT FOR EACH OF THE THREE GATES ARE ALSO LISTED

Case #	H	\bar{D}	O_1	O_2	O_3
1	0	0	1	1	1
2	0	1	1	0	0
3	1	0	0	0	0
4	1	1	0	1	1

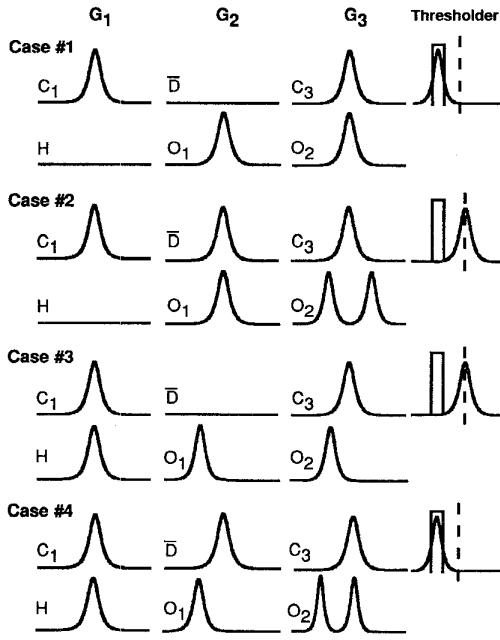


Fig. 3. A gate-by-gate illustration of the ideally expected physical behavior of the pulses in all four possible logical cases.

of the ideal physical behavior is shown in Fig. 3. In Fig. 3, we show the inputs to all the gates.

Case 1—($H = 0, \bar{D} = 0$): This case is physically the simplest. The header pulse is absent; so, the clock pulse C_1 undergoes no time shift in G_1 and O_1 is just C_1 with a time delay. Similarly, there is no code pulse; so, the output of G_2 is just C_1 with a further delay. Finally, C_1 and C_3 both enter the trapping gate G_3 . They should be synchronized when they enter G_3 , and they should have roughly the same amplitude. The two pulses self-trap, shifting the frequency of C_3 into the window of the discriminator and registering a nonzero value at the threshold.

Case 2—($H = 0, \bar{D} = 1$): In this case, as before, the absence of a header pulse implies that O_1 is just the clock pulse C_1 . However, this pulse then interacts with the code pulse in G_2 since they are synchronized, and both pulses are shifted out of their timing windows. Thus, neither is coincident with C_3 in G_3 so that C_3 is not shifted in frequency, and the threshold registers no energy. Since the pulse C_3 undergoes a complete collision with one of the two pulses in O_2 , it is imperative

that this collision be as symmetric as possible, so that the integrated frequency shift over the entire collision is as close to zero as possible.

Case 3—($H = 1, \bar{D} = 0$): A header pulse is present in this case; so, it shifts the clock pulse C_1 out of its timing window. However, there is no code pulse in this case; so, $O_2 = O_1$ with the same time shift. Consequently, the output O_2 is not synchronized with the clock pulse C_3 and undergoes no frequency shift, and the threshold registers no energy.

Case 4—($H = 1, \bar{D} = 1$): The header pulse is once again present so that C_1 is shifted out of its timing window. Consequently, although \bar{D} is present, the O_1 and \bar{D} pulses do not interact and remain in their time slots. When they are combined in O_2 , the portion of O_2 that is due to \bar{D} is synchronized with C_3 in G_3 so that C_3 is trapped and undergoes a frequency shift. Consequently, the threshold measures energy.

It is not trivial to obtain the ideal behavior just outlined because the pulses are not ideal solitons, and their nonlinear evolution in the optical fibers is quite complicated. We will show in our simulations that the desired behavior can be obtained with reasonable contrasts between the 1's and the 0's, but the parameter regime of operation must be carefully chosen.

IV. DESIGN ISSUES

The normalized equations that we are using to model the propagation of the light pulses through the gates (1) have time normalized with respect to the pulse duration, τ . The highest bit rates are achieved by using pulses with the shortest possible durations. An absolute lower limit of about 500 fs is set by the Raman effect. It is important that the pulses be solitons in the second length of fiber in the dragging gates so that they can shift as a unit out of their timing window. The peak power of the soliton P_{sol} is then given in terms of the fiber parameters by the formula [10]

$$P_{\text{sol}} = 0.777 \frac{\lambda^3 A_{\text{eff}} D}{\pi^2 c n_2 \tau^2} \quad (2)$$

and the soliton period which is the dispersive scale length is given by

$$Z_0 = 0.322 \frac{\pi^2 c \tau^2}{\lambda^2 D} \quad (3)$$

where $n_2 = 3.2 \times 10^{-16} \text{ cm}^2/\text{W}$ is the Kerr coefficient of the fiber, λ is the wavelength which is set about $1.5 \mu\text{m}$, and c is the speed of light. The effective area of the fiber A_{eff} is typically about $50 \mu\text{m}^2$, and D is the dispersion which is in the range 1–17 ps/nm-km, depending on whether or not dispersion-shifted fiber is used. It is advantageous to reduce P_{sol} because that reduces the required laser power, but it is also useful to reduce Z_0 because the required length of fiber in the gates is a multiple of Z_0 and reducing Z_0 reduces the latency. As (2) and (3) make clear, these two desiderata are in conflict. Typical values of pulse energies are tens of picojoules, while typical values for Z_0 are about 15–500 m depending on the value of D . Since, as we will show, the required propagation length is 20–30 Z_0 , a typical length for this fiber is several

hundred meters, corresponding to a latency on the order of 10 μ s. This latency is large enough to restrict the use of soliton dragging gates to feed-forward architectures like the one being considered here.

In the first length of the fiber where the partial soliton collision takes place, the length is less critical than in the second fiber. However, the birefringence strength is critical because it must be large enough to lead to a significant frequency shift but not so large that the pulses in the two polarizations walk off before there is a substantial nonlinear interaction or the trapping threshold becomes too high. As discussed in the next section, the required value of δ is restricted to the range $\delta = 0.5 - 1.0$. The formula used to determine δ is [1]

$$\delta = \frac{\pi \Delta n (\tau / 1.76)}{\lambda^2 D}. \quad (4)$$

If nondispersion-shifted fiber is used, then $D = 17$ ps/nm-km and $\Delta n \simeq 10^{-5}$. This birefringence is quite small for polarization-maintaining fibers, and if dispersion-shifted fiber is used to reduce the power requirements, then Δn becomes even smaller. Maintaining polarization over the length necessary to shift the soliton frequencies in the first fiber is a serious experimental problem and is one of the most important factors impacting the reliability of these gates. Highly birefringent fiber is used in the second length of fiber so that polarization is maintained. In numerical simulations, however, there is no problem in maintaining polarization, so that the δ -value in the second length of fiber has no importance in the numerical simulations.

Having discussed the physical pulse parameters and their relationship to the normalized parameters, we now discuss the normalized parameters that we will be varying and their impact on system performance.

- 1) *Length of the Fiber Gates:* The processing speed of the CMLM depends upon the length of the gates. The average bit-rate for a ring network depends in turn on the bandwidth of the switch. The goal is to reduce the total length of the fiber in the gate as much as possible to minimize the latency while still maintaining a good contrast ratio between 1's and 0's. The first dragging gate in which the header pulse (H) transfers its characteristics to the clock pulse (C_1) is the most important as it strongly affects the outcome in the following gates. In this paper, when we refer to the gate length, we will always mean the sum of the lengths of the switching and high birefringence fiber.
- 2) *Pulse Amplitudes:* The amplitudes must be carefully chosen so that the radiation produced during pulse interactions is minimized, so that sufficient temporal shifts in the dragging gates and frequency shifts in the trapping gates are obtained, and so that the pulses are not excessively distorted. We will show that the range of allowed amplitude values is quite restrictive.
- 3) *Size and Position of the Spectral Window of the Threshold:* Both the size and position of the spectral window of the threshold impact the contrast ratio, and we determine optimal values in our simulations.

- 4) *Timing jitter:* Timing jitter can have a significant impact on the contrast ratio because both dragging and trapping depend sensitively on the initial temporal separation of the two pulses. We will determine the change in contrast ratio due to timing jitter.

V. SIMULATION AND RESULTS

In this section, we present our simulations of pulse propagation in the code-matching logic module (CMLM) for the four cases described in Section III.

The initial pulses in the first gate G_1 have the form

$$u(\xi = 0, s) = A_{10} \operatorname{sech}[(s + s_0)/W_{10}] \quad (5)$$

$$v(\xi = 0, s) = A_{20} \operatorname{sech}[(s - s_0)/W_{20}] \quad (6)$$

where A_{10} and A_{20} are the initial pulse amplitudes, W_{10} and W_{20} are the initial pulse widths, and $2s_0$ is the initial separation. The u -pulse corresponds to the control pulse and is along the fast axis, while the v -pulse corresponds to the signal pulse and is along the slow axis of the fiber. We are assuming that the initial widths are the same, i.e., $W_{10} = W_{20} = 1$, and for now we are also assuming that the initial positions are the same, i.e., $s_0 = 0$, which is equivalent to ignoring the effect of timing jitter. Later in this section, we will discuss the effect of varying s_0 . In the subsequent gates G_2 and G_3 , we set

$$u(\xi = 0, s) = A_{10} \operatorname{sech}(s) \quad (7)$$

and $v(\xi = 0, s)$ is given by the output of the previous gate, appropriately delayed.

In the dragging gate G_1 , we set $\delta = 0.5$ which is sufficiently small to ensure a long enough length for the nonlinear interaction. In the XOR dragging gate G_2 , we set $\delta = 0.75$ because at lower values of δ the pulses in the two different polarizations have sufficient energy to trap when they are synchronized. If the value of δ in a dragging gate is changed by $\Delta\delta$, a corresponding change of $\Delta\delta L/\delta$ in the length of the gate L will leave the time shift of the gate unchanged because the shift in central frequency of the control pulse $\Delta\omega_c$ of a dragging gate is proportional to $1/\delta$ [7]. In the trapping gate G_3 , we set $\delta = 0.5$ which numerical experimentation indicates is the largest reasonable value at which trapping occurs. At higher values of δ the threshold amplitude for trapping increases. Lower values of δ imply smaller birefringence which worsens the problems of polarization-holding.

In the first gate G_1 , the control pulse is the clock pulse C_1 . We set $A_{10} = 1.0$ when $C_1 = 1$ because it is critical that this pulse be a soliton. This pulse goes through all three gates; in Case 1, it must trap with the clock pulse C_3 , and in Case 4 it is present with both the code pulse \bar{D} and the clock pulse C_3 , and it must not overlap with any of these pulses as shown in Fig. 3. Thus distortion of C_1 has very deleterious effects, and numerical experiments show that the allowed amplitude range is $\simeq 0.95-1.05$. We set $A_{20} = 0.5$ when $H = 1$ which is less than A_{10} as would be expected but is large enough so that during the interaction the pulse does not distort much. This value is not critical but the required length of G_1 does depend on this choice. As we will show shortly, it is critical for this length to be long enough to ensure that the pulse

C_1 is sufficiently shifted in time, and that implies a length of $20Z_0$ for G_1 with our choice of parameters. With higher values of A_{20} the required fiber length is less, but the pulse C_1 undergoes more distortion and becomes less soliton-like.

In the second gate G_2 , we set

$$u(\xi = 0, s) = A_{10} \operatorname{sech}(s) \quad (8)$$

while $v(\xi = 0, s)$ is given by O_1 , appropriately time-shifted. We set $A_{10} = 1.0$ when $\bar{D} = 1$ and $A_{10} = 0$ when $\bar{D} = 0$ since this pulse is the control pulse and using the exact soliton amplitude minimizes the distortion during the interaction in G_2 . More importantly, the amplitude of this pulse should be as close to that of C_1 as possible. The C_3 pulse traps the \bar{D} pulse in Case 4 and the C_1 pulse in Case 1, and it is imperative that the interactions in the trapping gate G_3 are identical in the two cases in order to fix the parameters of the trapping gate, the threshold, and the location and size of the measurement window. The length of the second gate G_2 is not critical. In Case 2 when $H = 0$ and $\bar{D} = 1$, the two pulses O_1 and \bar{D} interact in G_2 and are shifted out of their timing window so that neither of them is synchronized with C_3 in G_3 . Numerical experimentation shows that a length of $10Z_0$ in the second gate is sufficient for this purpose. In Cases 1, 3, and 4 there should be no interaction in G_2 ; so, the length is of no importance in these three cases.

In the third gate G_3 , it is desirable for the amplitude of the O_2 pulse to be the same as that of the C_3 pulse. As we will describe shortly, we investigated a range of parameters, and we found that $A_{10} = A_{20} \simeq 0.87$ is optimal. We also show that the optimal length for the gate G_3 is about $4Z_0$ as we will discuss in detail. Another important issue in obtaining a good contrast ratio is the size and location in the frequency domain of the detection window for the threshold. Our simulations indicate that a detection window with a size equal to $0.6\Delta\omega$ where $\Delta\omega$ is the spectral width of the soliton pulse and centered at $1.0\Delta\omega$ away from the central frequency of an unshifted pulse is optimal.

A. Location and Size of the Window

When two pulses self-trap in a birefringent fiber, they shift each other's central frequency so that they move together. Therefore, the measurement window should be placed close to the shifted frequency in order to capture the central portion of the trapped pulse. For $A_{10} = A_{20} = 0.87$ and $W_{10} = W_{20} = 1$, the frequency shift is approximately $0.8\Delta\omega$. However, we center the measurement window at $1.0\Delta\omega$ because from our simulations we found that for a measurement window placed closer to the unshifted frequency than $1.0\Delta\omega$, the power in the window when $O_3 = 0$ increases due to the presence of the unshifted pulse, thus decreasing the contrast ratio.

We experimented with different sizes of the measurement window and found that a window of size $0.6\Delta\omega$ yields the best result. For a broader window, we find that when $O_3 = 0$ the energy of the unshifted pulse begins to enter the measurement window, and the contrast ratio decreases. For a narrower window, we find that when $O_3 = 1$, the energy in the window decreases and will make the result more susceptible to

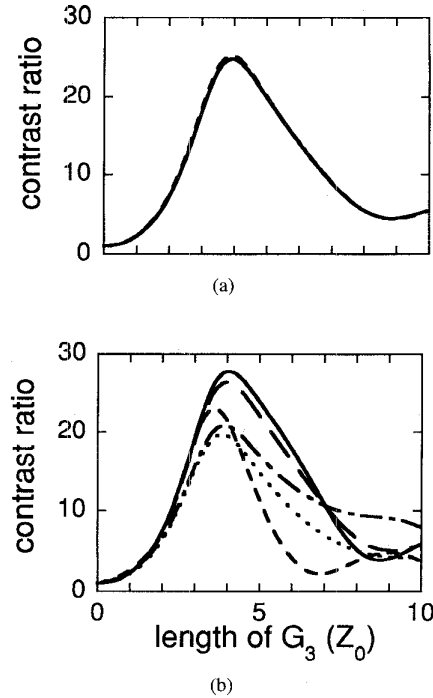


Fig. 4. Contrast ratio plotted as a function of the length of gate G_3 for different lengths of gate G_1 . (a) The contrast ratio is for a final output of $O_3 = 1$ obtained by simulating Case 1 from Table II versus a final output of $O_3 = 1$ obtained by simulating Case 3 from Table II. (b) The contrast ratio is for a final output $O_3 = 1$ obtained by simulating Case 4 from Table II versus a final output $O_3 = 0$ obtained by simulating Case 3 from Table II. Different lengths of the gate G_1 are represented by: Dashed curve, $12.5Z_0$; Dotted-dashed curve, $15.0Z_0$; Dotted curve, $17.5Z_0$; Solid curve, $20.0Z_0$; Long-dashed curve, $21.0Z_0$. Note that all curves are the same.

fluctuations due to noise, timing jitter, and amplitude variation. The system performance, however, is not sensitive to small changes in the choice of location and size of the timing window.

We now show detailed numerical simulations of the device behavior for the following critical parameters: 1) length of gate G_1 , 2) length of gate G_3 , and 3) pulse amplitudes in gate G_3 , and the effect of timing jitter.

B. Length of Gate G_1

Fig. 4(a) and (b) shows the contrast ratio as a function of the length of gate G_3 for two combinations of the four logical cases. We recall that the length reported here is the sum of the length of the switching and high birefringence fibers. In Fig. 4, we plot the contrast ratio versus the length of gate G_3 for lengths of gate G_1 from $12.5Z_0$ to $21Z_0$. The contrast ratio is defined as the ratio of the power measured when output $O_3 = 1$ to the power measured when output $O_3 = 0$.

In Fig. 4(a) the contrast ratio is obtained from Cases 1 and 3. From Fig. 3, we conclude that Cases 1 and 3 are similar as there are only two pulses at the input of gate G_3 . This combination is simpler to analyze because there are fewer interactions. As can be seen from Fig. 4(a), the contrast ratio is almost the same for lengths of G_1 from $12.5Z_0$ to $20Z_0$. In Case 1 in which $O_3 = 1$, there is no interaction in the

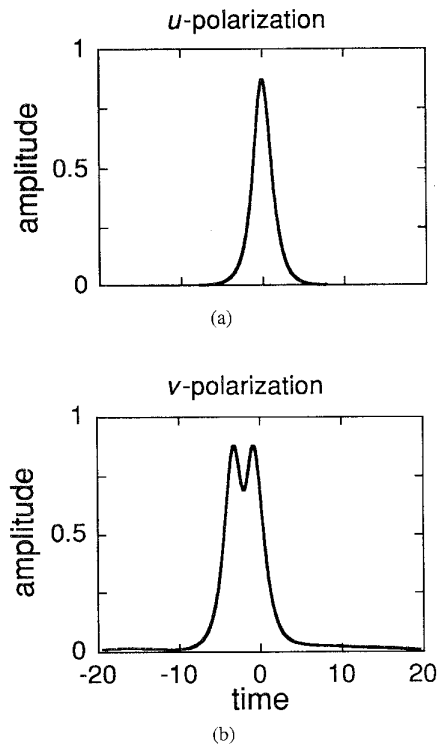


Fig. 5. Time domain plots of the input for Case 4 in gate G_3 . The length of gate G_1 is $12.5Z_0$ and $\delta = 0.5$. The length of gate G_2 is $10Z_0$ and $\delta = 0.75$.

first gate so that the length of the first gate does not matter. However, in Case 3 in which $O_3 = 0$, the C_1 pulse should be temporally shifted far enough so that it does not interact with the C_3 pulse. A maximum contrast ratio of 24.7 is achieved for all the lengths of G_1 considered when G_3 has a length $4.0Z_0$. Hence, for Case 3, a length of $12.5Z_0$ or more for G_1 is sufficient to perform the required logic.

In Fig. 4(b), we plot the contrast ratio obtained from Case 3 ($O_3 = 0$) and Case 4 ($O_3 = 1$) versus the length of gate G_3 for different lengths of gate G_1 . A final output $O_3 = 0$ is obtained in both Cases 2 and 3. In both cases the C_3 pulse does not shift from its initial location in the frequency domain. Hence, the required length of gate G_1 will be determined by Case 4 and not by any other case. Recall that in Case 4 $H = \bar{D} = 1$. The final output $O_3 = 1$ is obtained when C_3 is trapped by the \bar{D} pulse. Intuitively, one would expect the contrast ratio to improve with the length of the dragging gate G_1 . However, the contrast ratio first worsens as the length of G_1 increases from $12.5Z_0$ to $17.5Z_0$ before improving as the length increases from $17.5Z_0$ to $20Z_0$. The contrast ratios when the length of gate $G_1 > 20Z_0$ are larger than when the length of $G_1 < 20Z_0$. These observations can be explained as follows. Fig. 5(b) shows the input along the slow axis of gate G_3 for Case 4 when G_1 has a length of $12.5Z_0$. It is apparent that a length of $12.5Z_0$ for gate G_1 is not enough for the C_1 pulse to be sufficiently time shifted, so that when the C_1 pulse is polarization-combined with \bar{D} at the output of G_2 , the two pulses significantly overlap. Part of the C_1 pulse overlaps with the \bar{D} pulse at the input of gate G_3 . Also, the \bar{D} pulse is time-shifted due to the interaction in the XOR gate

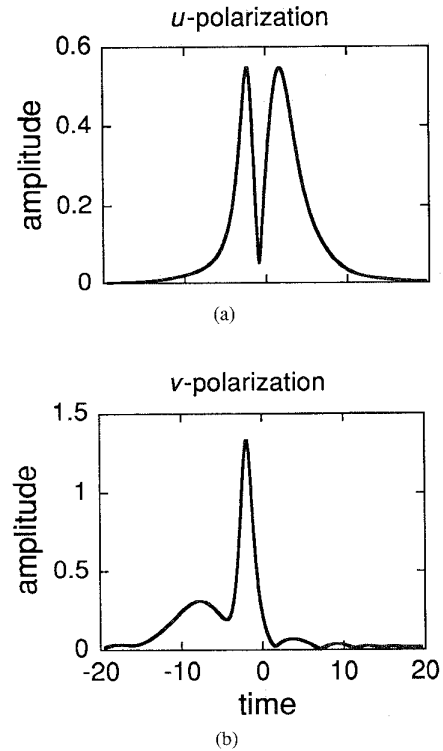


Fig. 6. Time domain plots of the input for Case 4 after propagating a distance $3.5Z_0$ in gate G_3 . The fiber and the pulse parameters are the same as in Fig. 5.

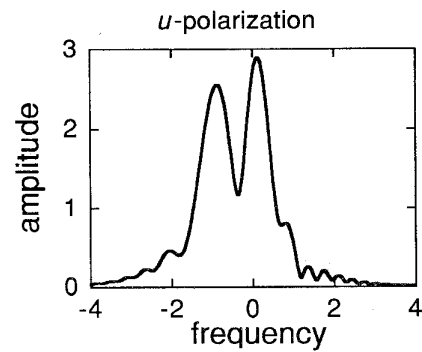


Fig. 7. Frequency domain plot of the C_3 pulse shown in Fig. 6.

G_2 , while ideally, in Case 4 there should be no interaction in gate G_2 . As the \bar{D} and the C_3 pulses trap in G_3 , part of the C_1 pulse is also trapped—as can be seen from the time domain plot of the pulses in Fig. 6(a) and (b). The energy contribution from C_1 causes a substantial frequency shift in the C_3 pulse even though \bar{D} is time-shifted and eventually results in a good contrast ratio. Observe that the C_3 pulse distorts significantly and is far from being a hyperbolic secant pulse in the frequency domain, as shown in Fig. 7. With the introduction of noise, amplitude jitter, and timing jitter the performance at this length of G_1 is likely to degrade.

As the length of gate G_1 is increased beyond $12.5Z_0$ in Case 4, the separation between the C_1 pulse and the \bar{D} pulse increases at the input of gate G_3 so that the C_1 pulse no longer overlaps with the \bar{D} pulse. However, the \bar{D} pulse is

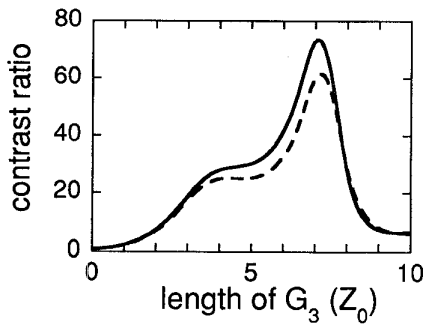


Fig. 8. Contrast ratio plotted as a function of the length of gate G_3 assuming that gate G_1 has a length of $20Z_0$. The two contrast ratioplots are for a final output $O_3 = 1$ obtained by simulating Cases 1 and 4 versus a final output of $O_3 = 0$ obtained by simulating Case 2. The parameter values are the same as those in Fig. 4. The solid curve, Case 4 versus Case 2; the dashed curve, Case 1 versus Case 2.

still time-shifted because the C_1 pulse is still temporally close to the \bar{D} pulse at the input of gate G_2 . This situation results in partial trapping of the \bar{D} pulse with the C_3 pulse in gate G_3 and a decrease in the frequency shift of C_3 . The contrast ratio therefore decreases. When the length is further increased, the time shift of \bar{D} by C_1 decreases, so that the contrast ratio increases and approaches the ideal case in which, for trapping purposes, the \bar{D} and C_3 pulses are temporally coincident and the C_1 pulse is not present. When the length of gate G_1 is $20Z_0$, the maximum contrast ratio obtained is ~ 27.8 at a length of $4Z_0$ along the trapping gate G_3 . At this length of gate G_1 , Fig. 4(a) and (b) appear almost identical. Further increase of the length of gate G_1 to $21Z_0$ in Fig. 4(b) leads to little change.

We conclude that the optimal length of gate G_1 is $20Z_0$ for the parameters chosen.

C. Length of Gate G_3

In Fig. 8, we plot the contrast ratios, fixing the length of the gate G_1 at $20Z_0$, for the two remaining combinations for contrast ratio—Cases 1 versus 2 and 4 versus 2. In Case 2, $H = 0$, and $\bar{D} = 1$ so that there is no interaction in gate G_1 and O_1 is just C_1 with a time delay. However, the O_1 pulse interacts with \bar{D} in G_2 because they are synchronized, and both pulses shift out of their respective timing windows. The input O_2 along the slow axis of gate G_3 is shown in Fig. 9. The four peaks are due to the dragging effect in the gate G_2 which results in the formation of shadows [4]—portions of the pulse along one polarization that get attached to the pulse along the other polarization. At the end of gate G_2 when the pulses are polarization-combined we must introduce a time delay in order for the pulse along the fast axis of gate G_2 to synchronize with the pulse along the slow axis of G_2 . Consequently, the shadows separate from the pulses to which they were originally attached. In Fig. 9, the first peak from the left is the shadow of the C_1 pulse, the second peak is C_1 itself, the third peak is the \bar{D} pulse, and the fourth peak is the shadow of \bar{D} .

Up until $4.0Z_0$ in gate G_3 , the curves in Fig. 8 are almost identical to the curves in Fig. 4 when the gate G_1 has a length of $20Z_0$. At longer lengths of gate G_3 , we find that in Case

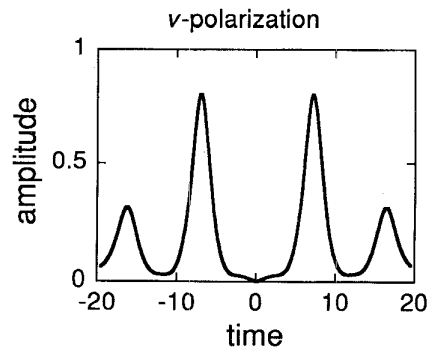


Fig. 9. Time domain plot of the pulse along the slow axis (v -polarization) at the input of gate G_3 for Case 2. The length of gate G_1 is $20Z_0$ and $\delta = 0.5$. The length of the gate G_2 is $10Z_0$ and $\delta = 0.75$.

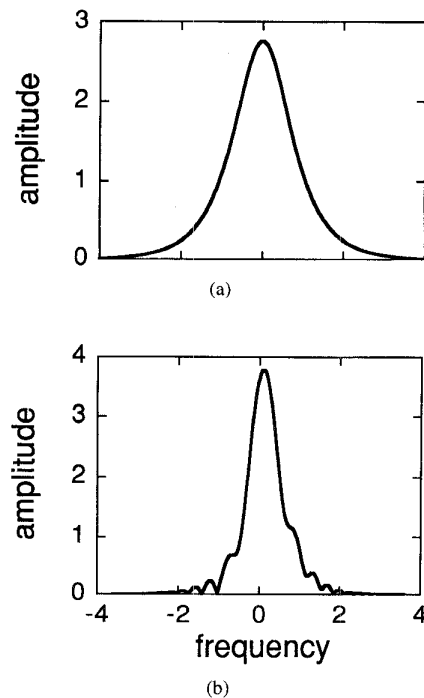


Fig. 10. Frequency domain plot of the clock pulse C_3 (a) at the input of gate G_3 , (b) at a distance of $7.0Z_0$ along gate G_3 . The initial pulse parameters are $A_{10} = 0.87$ and $W_{10} = 1.0$.

2, the C_3 pulse undergoes a complete collision with part of O_2 —the part due to the \bar{D} pulse. The C_3 pulse broadens and partially traps with the \bar{D} pulse. The broadening in the time domain leads to a narrowing of the pulse in the frequency domain. This reduction can be observed when we compare Fig. 10(a) with (b). Fig. 10(a) is the frequency domain plot of the C_3 pulse at the input of the gate G_3 , and Fig. 10(b) shows the same C_3 pulse at a length of $7.0Z_0$ along the gate G_3 .

Due to the contraction of the pulse in the frequency domain, the energy is pulled out of the measurement window and leads to a significant increase in the contrast ratio, but the contrast ratio in the other two combinations at a length of $7.0Z_0$ along gate G_3 has diminished to about 11. Fig. 11 summaries all the plots in Figs. 4 and 8. The length of gate G_1 is chosen to be $20Z_0$. The optimal length for gate G_3 is in the range of

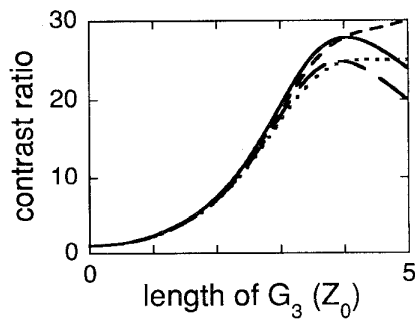


Fig. 11. Contrast ratio plotted as a function of the length of gate G_3 assuming that gate G_1 has a length of $20Z_0$. All the four possible contrast ratios are shown. Case 1 versus Case 2, dotted curve; Case 4 versus Case 2, dashed curve; Case 1 versus Case 3, long-dashed curve; Case 4 versus Case 3, solid curve.

$3.5\text{--}4.5Z_0$ and the maximum contrast ratio achieved, at these lengths of G_3 , for different logical cases is in the range of 24 to 27.

D. Pulse Amplitudes in Gate G_3

For $\delta = 0.5$, the amplitudes for trapping for pulses of the form of (5) and (6) with $s_0 = 0$ are $A_{10} = A_{20} = 0.87$, which are also the values chosen in the experiments conducted by Islam *et al.* [11]. If $A_{10} = A_{20} < 0.87$, the mutual shift in the central frequencies is not sufficient so that the pulses will eventually separate. However, if the amplitudes are close to the threshold for trapping, the two pulses will co-propagate a long distance before they separate. Above the trapping amplitude, the pulses will trap each other. For higher amplitudes, however, multiple peaks will form. We therefore choose the amplitude of C_3 to be 0.87. Note that for this choice of trapping amplitude, O_2 has to undergo a lumped loss before it can be used as the input to gate G_3 .

To possibly improve the contrast ratio, we varied the amplitude of the trapping pulses in gate G_3 . We considered two cases, one in which we reduced the amplitude from 0.87 to 0.75 and another in which we increased the amplitude to 0.95. In Fig. 12, the amplitude of the trapping pulses equals 0.75. We plot the contrast ratio as a function of the length of gate G_3 for all four combinations with the length of the gate G_1 fixed at $20Z_0$. In Fig. 12(a), we placed the measuring window near the peak of the shifted pulse, at about $0.7\Delta\omega$ away from the central frequency of an unshifted pulse. We find that in all cases, the location of the maximum has shifted. The maximum contrast ratio is nearly equal to 34 but occurs when gate G_3 has a length of about $9Z_0$. We can achieve high contrast ratios at a smaller length of gate G_3 if we move the measuring window to the same location as for trapping amplitudes equal to 0.87, which is $1.0\Delta\omega$ from the central frequency of an unshifted pulse. We find that a contrast ratio of about 34 is achieved when gate G_3 has a length of $5Z_0$. However, the power measured when the final output $O_3 = 1$ is only 30% of the power when the measurement window is located at $0.7\Delta\omega$ spectral widths. At $1.0\Delta\omega$, the window is actually located at the trailing edge of the pulse and not close to the peak of the pulse.

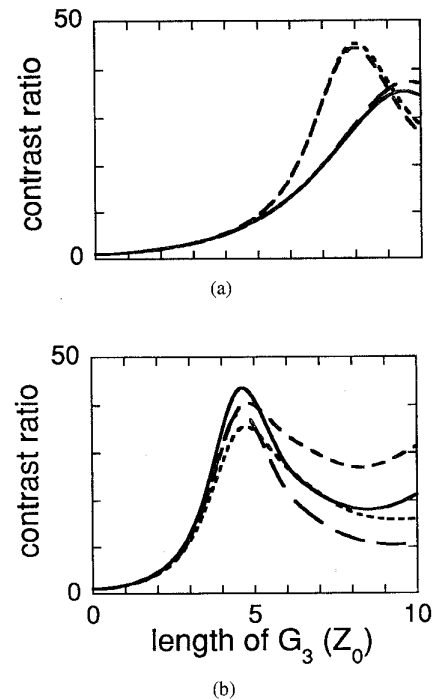


Fig. 12. Contrast ratio plotted as a function of the length of gate G_3 with the length of gate G_1 fixed at $20.0Z_0$. Parameters used for the fiber and the window are the same as in Fig. 11, except that the initial amplitude of C_3 has been changed to 0.75 and the measuring window is centered at (a) 0.7 soliton spectral widths and (b) 1 soliton spectral widths away from the center of an unshifted pulse. Case 1 versus Case 2, dotted curve; Case 4 versus Case 2, dashed curve; Case 1 versus Case 3, long-dashed curve; Case 4 versus Case 3, solid curve.

The contrast ratio measured when $A_{10} = A_{20} = 0.75$ is larger by a factor of 30% than when $A_{10} = A_{20} = 0.87$, but the required length of gate G_3 doubles. Smaller trapping pulses give higher contrast ratios because the effect of the pulse in one polarization on the shape of the pulse in the other polarization decreases with pulse intensity. High intensity pulses distort each other much more, resulting in a double peak in the spectrum and energy transfer into the wings.

In Fig. 13, we show results when the trapping amplitude is increased to 0.95. In Fig. 13(a), the measurement window is centered at $1.0\Delta\omega$ away from the central frequency of an unshifted pulse, while in Fig. 13(b) it is centered at $1.25\Delta\omega$ away. The maxima for some of the curves are lower than those when the trapping amplitude is 0.87. Higher peaks are observed in two of the cases at a length of $7.5Z_0$ just like in Fig. 8. The curves in Fig. 13 are almost identical to those of Fig. 11, but the contrast ratios are worse because of the tendency of higher-intensity pulses to break up and distort leading to fluctuations, broadening, and multiple peaks in the frequency domain. When we set the trapping pulse amplitude to $A_{10} = 1.0$, the pulse shape evolves in a complex way and the contrast ratio is worse.

We conclude that trapping amplitudes greater than about 0.9 lead to a deterioration of the contrast ratio. Trapping amplitudes lower than 0.85 but higher than about 0.75 improve the contrast ratio slightly but lead to significantly longer lengths of gate G_3 .

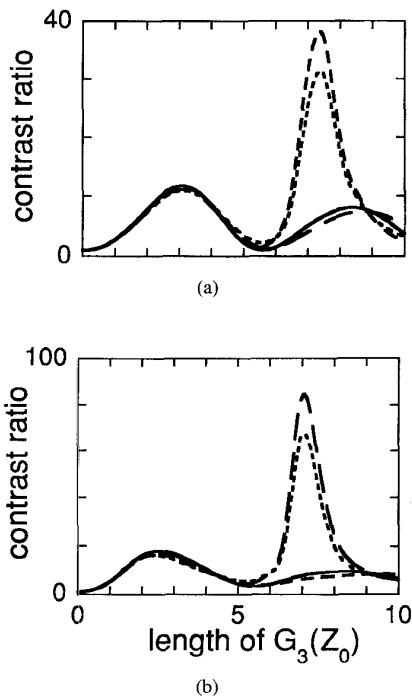


Fig. 13. (a) Contrast ratio plotted as a function of the length of gate G_3 , with the length of gate G_1 fixed at $20.0Z_0$. Parameters used for the fiber and the window are the same in Fig. 11, except that the initial amplitude of C_3 has been changed to 0.95. In (b), the spectral window is centered at 1.25 soliton spectral widths away from the center of an unshifted pulse. Case 1 versus Case 2, dotted curve; Case 4 versus Case 2, dashed curve; Case 1 versus Case 3, long-dashed curve; Case 4 versus Case 3, solid curve.

E. Effect of Timing Jitter

In the simulations that have been presented up to this point, we determined within the parameter space examined the best design parameters under ideal conditions. Perturbative factors such as noise, amplitude jitter, and timing jitter, were ignored. Timing jitter, in particular, can have significant impact on the performance of CMLM because the frequency shift due to the dragging effect depends sensitively on pulse synchronization. Moreover, timing jitter at the input of the first gate can affect the output of all subsequent gates. At the extreme, a final output of 1 can be mistaken for a 0, or a final output of 0 can be mistaken for a 1. Since trapping is particularly sensitive to pulse synchronization, a final output of 1 is expected to be more drastically affected by timing jitter than a final output of 0. The jitter most likely occurs in the header pulse H because it comes from the ring network. However, C_1 , \bar{D} , and C_3 can also have jitters because of the jitter in the laser sources. To estimate the effect of timing jitter we plot in Figs. 14–17 the variation of the output power in the measurement window for all four cases using the optimal parameters determined in the previous sections for the pulses and the logic modules. The length of $G_1 = 20Z_0$, the length of $G_2 = 10Z_0$, and the length of $G_3 = 4.0Z_0$. The pulse and fiber parameters are exactly the same as those used for the plots in Fig. 11. The measurement window is centered at $1.0\Delta\omega$ away from the central frequency of an unshifted pulse, and it is $0.6\Delta\omega$ wide.

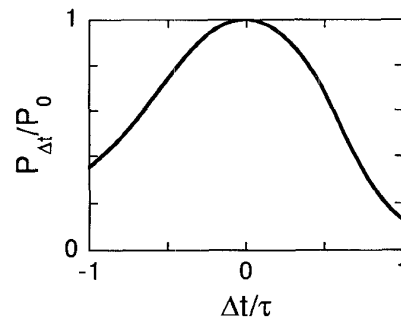


Fig. 14. The normalized power $P_{\Delta t}/P_0$ of the O_3 pulse is plotted as a function of the normalized timing jitter $\Delta t/\tau$ of the C_1 pulse. A final output $O_3 = 1$ is obtained by simulating Case 1 from Table II. Δt is the timing jitter, τ is the pulse width, $P_{\Delta t}$ is the power measured when timing jitter equals Δt , and P_0 is the power measured when $\Delta t = 0$.

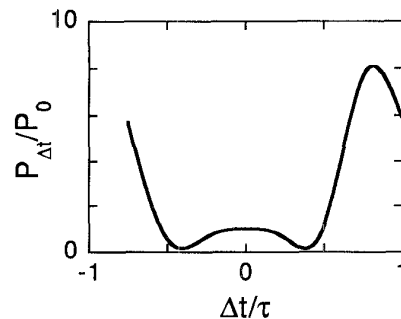


Fig. 15. The normalized power $P_{\Delta t}/P_0$ of the O_3 pulse is plotted as a function of the normalized timing jitter $\Delta t/\tau$ of the C_1 pulse. A final output $O_3 = 0$ is obtained by simulating Case 2 from Table II. Δt is the timing jitter, τ is the pulse width, $P_{\Delta t}$ is the power measured when timing jitter equals Δt , and P_0 is the power measured when $\Delta t = 0$.

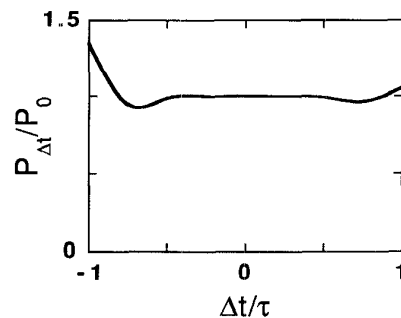


Fig. 16. The normalized power $P_{\Delta t}/P_0$ of the O_3 pulse is plotted as a function of the normalized timing jitter $\Delta t/\tau$ of the H pulse. A final output $O_3 = 0$ is obtained by simulating Case 3 from Table II. Δt is the timing jitter, τ is the pulse width, $P_{\Delta t}$ is the power measured when timing jitter equals Δt , and P_0 is the power measured when $\Delta t = 0$.

In Fig. 14, we consider Case 1. The expected output is $O_3 = 1$. Since there is no header pulse, we assume that the C_1 pulse is jittered when it arrives at gate G_3 . We plot the normalized power of the O_3 pulse detected in the measurement window $P_{\Delta t}/P_0$ versus the normalized timing jitter $\Delta t/\tau = \Delta s_0/1.76$ where Δt is the timing jitter, τ is the FWHM pulse width, $P_{\Delta t}$ is the power measured when timing jitter equals Δt , and P_0 is the power measured when $\Delta t = 0$. From Case 1 of Fig. 3, the output $O_3 = 1$ results from the trapping of two orthogonally

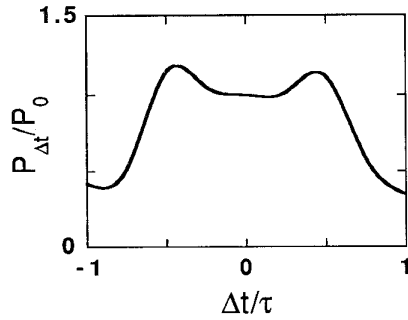


Fig. 17. The normalized power $P_{\Delta t}/P_0$ of the O_3 pulse is plotted as a function of the normalized timing jitter $\Delta t/\tau$ of the H pulse. A final output $O_3 = 1$ is obtained by simulating Case 4 from Table II. Δt is the timing jitter, τ is the pulse width, $P_{\Delta t}$ is the power measured when timing jitter equals Δt , and P_0 is the power measured when $\Delta t = 0$.

polarized pulses in G_3 . The jittering in the arrival time of C_1 results in the jittering of O_1 , hence the pulses at the input of G_3 are not synchronized and the overlap between the two pulses decreases. Consequently, the portion of the pulses that are trapped and the resulting frequency shift also decrease and the measured power decreases. From Fig. 14, when $|\Delta t/\tau| = 0.5$, $P_{\Delta t}/P_0 \approx 0.7$.

In Fig. 15, we consider Case #2. The expected output is $O_3 = 0$. Again, since there is no header pulse, we assume that there is a timing jitter in the C_1 pulse. We plot the normalized power of the O_3 pulse detected in the measurement window versus the normalized jitter of the C_1 pulse. From Case 2 of Fig. 3, the output $O_3 = 0$ results from a lack of trapping between the clock pulse C_3 with either of the two pulses in O_2 . The jittering in C_1 results in the jittering of O_1 , so that O_1 is not synchronized with \bar{D} at the input of G_2 . Their mutual frequency shift decreases such that their temporal separation at the input of G_3 decreases. In Case 2, the C_3 pulse always collides with the \bar{D} pulse after propagating some distance along gate G_3 . The interaction causes C_3 to change shape and shift in frequency. When the temporal position of the \bar{D} pulse at the input of G_3 changes, the location of the collision also changes. Since we fix the length of gate G_3 at $4Z_0$, the power detected in the measurement window depends upon the extent of the interaction that has taken place until then and upon the shape of the C_3 pulse at that point. From Fig. 15, when $|\Delta t/\tau| < 0.25$, the power measured actually decreases thus improving the contrast ratio. However when $|\Delta t/\tau| > 0.25$, the jitter in O_1 is so large that the input at G_2 begins to resemble that of Case 4. The temporal separation between C_3 and \bar{D} at the input of G_3 decreases and the power measured increases.

In Fig. 16, we consider Case 3 where $H = 1$ and $\bar{D} = 0$. We assume that the H pulse is jittered at the input of gate G_1 . The expected output is $O_3 = 0$. We plot the normalized power of the O_3 pulse detected in the measurement window versus the normalized jitter of the H pulse. From Case 3 of Fig. 3, the clock C_1 and the header pulse H are not synchronized at the input of gate G_1 because of the timing jitter in H . The overlap between the two pulses decreases and their mutual frequency shift decreases. As a result, the temporal separation between

O_2 and C_3 at the input of G_3 decreases. From Fig. 16, when $|\Delta t/\tau| < 0.5$, O_2 and C_3 are still sufficiently far apart that they do not interact, hence the power measured in O_3 does not change. When $0.5 < |\Delta t/\tau| < 0.7$, the power measured decreases for the same reason that the power measured in Case #2 first decreases when $|\Delta t/\tau|$ increases from zero. However when $|\Delta t/\tau| > 0.7$, the input to G_3 resembles that of Case 1. The pulses in O_2 and C_3 begin to trap each other and the power measured increases.

In Fig. 17, we consider Case 4 where $H = 1$ and $\bar{D} = 1$. We again assume that the H pulse is jittered. The expected output is $O_3 = 1$. We plot the normalized power of the O_3 pulse detected in the measurement window versus the normalized jitter of the H pulse. As in Case 3, the clock pulse C_1 and the header pulse H are not synchronized at the input of gate G_1 because of the timing jitter in H . Therefore, the temporal separation between O_1 and \bar{D} at the input of G_2 decreases. From Fig. 17, when $|\Delta t/\tau| < 0.25$, O_1 and \bar{D} are still sufficiently far apart that they do not interact, hence the trapping in G_3 is not affected and the power measured does not change. When $|\Delta t/\tau| > 0.25$, O_1 begins to shift \bar{D} away from its time slot such that it is no longer synchronized with C_3 at the input of G_3 . As occurred in Case 2, we find that due to the interplay of the frequency shift, the change in the pulse shape, and observation at the fixed length of $4Z_0$ in G_3 , the power measured in O_3 increases when $0.25 < |\Delta t/\tau| < 0.4$. However when $|\Delta t/\tau| > 0.4$, the input to G_3 resembles that of Case 2, and the power measured steadily decreases.

In summary, if $|\Delta t/\tau| \leq 0.5$, the performance of the CMLM is more or less unaffected. The measured contrast ratio decreases by at worst 30%. The degradation is mainly due to the decrease in the power measured in Case 1. The power measured in the other cases are either unaffected or actually improve. However, for $|\Delta t/\tau| \geq 0.7$, the performance of the CMLM degrades considerably.

Islam [6] reported that the timing window of the dragging gate can be widened by a factor of 1.5 to 2 by introducing a prechirper or a lumped gain to asymmetricize the interaction during walk-off so that the control pulse will be chirped even in a complete collision. In either case, the complexity of the dragging gate increases. A prechirper will require higher energy in the switching pulse and a lumped gain will significantly distort the control pulse C_1 . Whether these techniques will relax the timing jitter restriction of the CMLM remains unclear.

VI. CONCLUSION

We have numerically simulated a code-matching logic module which is at the heart of a soliton ring network proposed by Sauer *et al.* [3]. We have studied several design issues that must be addressed before the soliton ring network can possibly be implemented. We found that the complex functions that the soliton logic gates are required to perform in the proposed logic module require fine-tuning of the design parameters. It is imperative for the clock pulse C_1 to be a perfect soliton because it has to travel through three cascaded gates. The optimal length of the first dragging gate G_1 is about $20Z_0$.

A sufficient length for the XOR gate G_2 is about $10Z_0$. The normalized birefringence δ of the fiber in the XOR gate G_2 should be 0.75 because for fiber with a lower birefringence, the pulse will self-trap in gate G_2 . We also find that the optimal length for the AND gate G_3 is in the range $3.5Z_0$ to $4.5Z_0$. The amplitude of the trapping pulses should be about 0.85 to obtain the best contrast ratio. The measurement window should be about $0.6\Delta\omega$. For a smaller window size, there is not enough energy in the window, and for larger window size the energy in the case of a 0 starts entering the window and decreases the contrast ratio. The measurement window should be placed at about $1.0\Delta\omega$ away from the location of the peak of an unshifted pulse.

With the above parameters, we obtain a best contrast ratio of 24 in our simulations. For a timing jitter of less than 0.5 pulse widths, the contrast ratio at worst decrease by 30%. For a timing jitter larger than 0.7 pulse width, the contrast ratio degrades considerably.

It should be noted that we have assumed perfect extinction between the two polarization eigenaxes. In practice, it is very difficult at the birefringence values required to maintain a good extinction ratio for more than a few minutes, so that maintaining polarization is an important experimental difficulty.

In conclusion, we find a parameter regime within which the code-matching module can operate successfully, but this parameter regime is quite narrow.

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